



Attorney's Docket No.: 13361-059001
Client's Ref. No.: MP0359

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Number of pages including this page 6

Applicant : Swee-Ann Teo et al.
Serial No. : 10/738,368
Filed : December 15, 2003

Art Unit : 2816
Examiner : Jackson, Blane J

Title : Sigma Delta Modulated Phase Lock Loop with Phase Interpolation

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Attached to this facsimile communication cover sheet is Response to Notice of Allowance, Part B – Fee Transmittal, Comments on Examiner's Reasons for Allowance and Submission of Credit Card Payment, faxed this 10th day of Jan, 2007, to the United States Patent and Trademark Office.

Date: 1/10/07

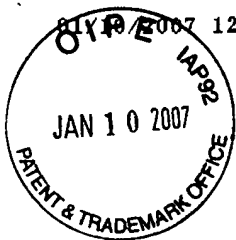
Respectfully submitted,

Mark D. Kirkland
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Swee-Ann Teo et al.
Serial No. : 10/738,368
Filed : December 15, 2003
Title : SIGMA DELTA MODULATED PHASE LOCK LOOP WITH PHASE INTERPOLATION

Art Unit : 2618
Examiner : Jackson, Blane J
Confirmation No.: 9617
Notice of Allowance Date: 10/10/06

MAIL STOP ISSUE FEE

Commissioner for Patents
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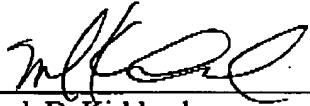
RESPONSE TO NOTICE OF ALLOWANCE

In response to the Notice of Allowance mailed April 10, 2006, enclosed are a completed issue fee transmittal form PTOL-85b, Comments on Examiner's Reasons for Allowance and a submission of Credit Card Payment for \$1400 for the required fee.

Please apply any additional charges or credits to our Deposit Account No. 06-1050.

Respectfully submitted,

Date: 1/10/07


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CERTIFICATE OF TRANSMISSION BY FACSIMILE

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1/10/2007
Date of Transmission


Signature

Suzanne M. Forno

Typed or Printed Name of Person Signing Certificate



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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Swee-Ann Teo et al.
Serial No. : 10/738,368
Filed : December 15, 2003
Title : SIGMA DELTA MODULATED PHASE LOCK LOOP WITH PHASE INTERPOLATION

Art Unit : 2618
Examiner : Jackson, Blane J
Confirmation No.: 9617
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COMMENTS ON EXAMINER'S REASONS FOR ALLOWANCE

Applicant recognizes that in accordance with M.P.E.P. § 1302.14, the Examiner's reasons for allowance need not set forth all of the details as to why the claims are allowed. In the above-referenced application, Applicant does not concede that the Examiner's stated reasons for allowance are the only reasons for which the claims are allowable. In particular, Applicant does not concede that all of the identified limitations—i.e., “the prior art made of record fails to teach a phase locked loop comprising a phase interpolator operable to receive one or more phase signals, each of the phase signals being delayed with respect to the output carrier signal, the phase interpolator operable to generate an interpolated output signal based in part on the dither control signal for controlling the frequency of the output carrier signal”—are included in each identified claim or necessary to distinguish over the prior art of record or to satisfy the requirements of 35 U.S.C. § 112. Furthermore, the claims may be patentable for other reasons. In addition, dependent claims are allowable on their own merits, and are allowable on the basis of a sub-combination of the recited features of the dependent claims and their respective base claims.

Please apply any additional charges or credits to our Deposit Account No. 06-1050.

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Applicant : Swee-Ann Teo et al.
Serial No. : 10/738,368
Filed : December 15, 2003
Page : 2 of 2

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Respectfully submitted,

Date: 1/10/07



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